Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A method for testing latch-up phenomenon of a chip, the chip being tested on a test platform, the test platform storing a test program of the chip for testing the chip, the method comprising:

(a)obtaining the test program of the chip tested on the test platform;

(b)obtaining pin data of the chip by the test program of the chip;

(c)setting up an input pin of the chip with an initial value; and

(d)providing a test current to the pin of the chip, and then measuring the current between a power end and a ground end of the chip to see if it exceeds a first predetermined value.

[c2] 2.The method of claim 1 further comprising:

(e)Using another test current having a higher value to repeat Step(d), until the test current exceeds a second predetermined value.

[c3] 3.The method of claim 1 wherein Step(d) further comprises providing the test current to each of the pins, and

measuring the current between the power end and the ground end of the chip to see if it exceeds the first predetermined value.

[c4] 4. The method of claim 1 further comprising determining that the chip not pass the latch-up test if the test current exceeds the first predetermined value.

[c5] 5. The method of claim 2 further comprising determining that the chip pass the latch-up test if the test current used in Step(e) exceeds the second predetermined value, and the current between the power end and the ground end of the chip does not exceed the first predetermined value.

[c6] 6. A device for implementing the method of claim 1.

[c7] 7. A test platform for testing latch-up phenomenon of a chip comprising:
a memory;
a parameter measurement unit (PMU) for providing a current source to the chip and measuring the current between a power end and a ground end of the chip;
a latch-up test program stored in the memory comprising:
a path setup program code for obtaining a test program of the chip;

a pin setup program code for obtaining a pin of the chip by the test program of the chip;
an initial setup program code for setting the input pin of the chip with an initial value;
a current measuring setup program code for driving the PMU to measure the current between the power end and the ground end of the chip; and
a current providing setup program code for driving the PMU to provide a test current to the pin of the chip; and
a processor for executing programs stored in the memory.

[c8] 8. The test platform of claim 7 wherein the test program is stored in the memory for testing the chip.

[c9] 9. The test platform of claim 7 wherein the chip comprises a plurality of I/O pins and a plurality of power pins.

[c10] 10. The test platform of claim 7 wherein the initial value is 0 or 1.

[c11] 11. The test platform of claim 5 being an automated test equipment (ATE).